Amendments to the Specification

Please amend paragraph [34] as follows:

[34] Figure 3 is a block diagram of an FGS encoder in accordance with one embodiment of the present invention. The encoder includes a first quantizer 300, a second quantizer 301, an inverse quantizer 302, and a number of subtracter circuits. The first quantizer ~~performs a DCT on a motion-compensated image and quantizing a result value~~ quantizes a resulting DCT value from a motion-compensated image. The second quantizer 301 re-quantizes (Q_2^{-1}) the value (x(k)) obtained by the first quantizer. The inverse-quantizer 302 ~~re-quantizes~~ inverse quantizes a value ($y_1(k)$) re-quantized by the second quantizer 301. A first subtracter 306 obtains a difference between a value ($Ny_1(k)$) of N times the re-quantized value ($y_1(k)$) and the inverse-quantized value ($\tilde{\chi}(k)$). A second subtracter 307 obtains a difference between the value (x(k)) quantized by the first quantizer 300 and the value quantized by the inverse-quantizer. And, a third subtracter 308 subtracts the output value of the first subtracter from the output value obtained by the second subtracter. The encoder also includes a maximum value calculating unit 304 for searching a maximum value from output values of the third subtracter, and a bit plane variable length coding unit 305 for performing variable length coding on the obtained maximum value by bit planes.